A CMOS Image Sensor with Pixelwise Triple-CG Modulation and Gain-Regulating Pre-ISP for Single-Frame Adaptive TCG-HDR Imaging

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***Abstract* — High dynamic range (HDR) imaging is a must-have feature in flagship mobile CMOS image sensors (CISs). Recently, pixels with triple conversion gains (CGs) are unveiled to enable triple-CG (TCG) HDR imaging. In this paper, we present a CIS design with on-chip CG modulator (CGM) and a dedicated image signal processor (pre-ISP) for adaptive TCG-HDR imaging. The CGM module containing pixel CG selection (CGS) blocks is in charge of pixel's CG determinations and producing pixel CGS data. Pixels receive CG-mode signals and perform a single full-bit-depth readout with their own CGs. Both the pixel CGS data and the full-bit-depth image data are collected by the pre-ISP to produce HDR images. A prototype CIS chip consists of 640 × 320 TCG pixels has achieved a dynamic range of 89dB when applying adaptive TCG-HDR imaging. At a frame rate of 60fps, the power consumed in adaptive TCG-HDR imaging is 54% less than that in conventional TCG-HDR imaging. The presented CIS design and adaptive TCG-HDR imaging aim at low-power single-frame HDR imaging related applications in mobile cameras.**

I. INTRODUCTION

HDR imaging is an essential feature of high-end mobile cameras, offering unprecedented user experiences in image capture, video filming, and machine vision. Among different kinds of HDR imaging, multi-CG based single-frame HDR imaging is favorable in high-end CISs due to its advantages in image quality and immunity to motion artifacts. At present, dual-CG (DCG) based single-frame HDR imaging has been adopted in CISs [1]-[2]. To extend dynamic range further, TCG-HDR imaging is developed and available in recent flagship mobile CIS products [3]. As the HDR synthesis in DCG/TCG HDR imaging requires multiple pixel readouts (in different CG setups), CISs suffer from reduced frame rate and higher power consumption. With the limited power budgets and battery capacity in portable devices, user experience is adversely affected in HDR imaging related applications such as time-lapse photography and long-term HDR video filming. To overcome the aforementioned shortcomings, adaptive DCG-HDR imaging was introduced in our previous works [4]. By using in-pixel 1-bit dynamic random-access memory (DRAM) and column-parallel successive-approximation-register (SAR) based pixel-CG selectors, pixels are adaptively set in their unique CG mode. During the readout period, pixels are read out in either high CG (HCG) or low CG (LCG) followed by a single full-bit-depth analog-to-digital converter (ADC) operation. Such single pixel readout process effectively reduces the overall chip power consumption, the camera operates at its native frame rate and produces high-quality HDR images. In TCG-HDR imaging, on the other hand, pixels have three CGs (HCG, middle CG (MCG), and LCG) and require 2-bit CG-mode signals to select a specific CG. In consideration of shrinking pixel size and preventing crosstalk, previous designs using in-pixel DRAM buffers and SAR based pixel-CG selectors are unsuitable to realize adaptive TCG modulations. In this paper, we report a CIS design with on-chip CGM and pre-ISP to enable pixelwise TCG modulations and gain regulations. Without including in-pixel signal buffers, the CIS performs adaptive TCG-HDR imaging to facilitate low-power single-frame HDR imaging related applications to mobile cameras.

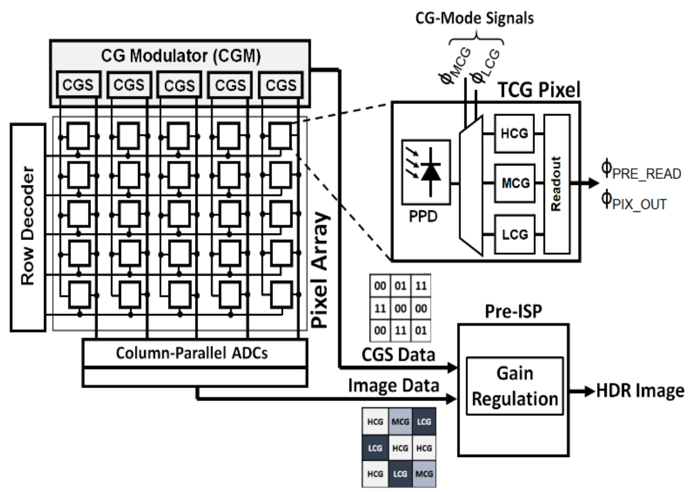

Fig. 1. Conceptual diagram of adaptive TCG-HDR imaging.

II. ADAPTIVE TCG-HDR IMAGING

Illustrated in Fig. 1 is a conceptual diagram of the proposed adaptive TCG-HDR imaging. The pixel is based on a typical

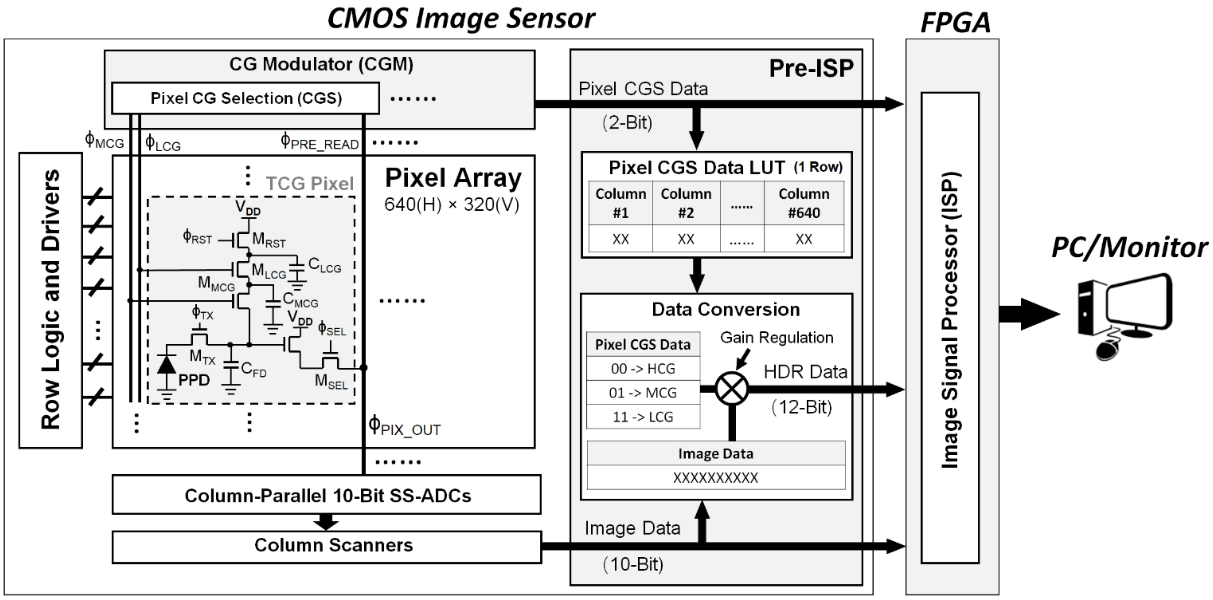

Fig. 2. Block diagram of the CIS architecture and the camera system. HDR images are synthesized by the on-chip pre-ISP.

TCG pixel backbone and has three CGs. According to the received CG-mode signal (formed by ϕ_{MCG} and ϕ_{LCG}), the pixel is set in one of the three CGs for readout. All CG-mode signals are determined by CGS blocks inside the CGM module and delivered to the pixel array in a column-parallel basis. When operating in a rolling shuttering scheme, the row decoder selects a specific row of pixels to receive their CG-mode signals. Pixel outputs (ϕ_{PRE_READ} and ϕ_{PIX_OUT}) are either sent to CGS blocks for CG-mode signal determinations or to column-parallel ADCs for image data synthesis. In adaptive TCG-HDR imaging, CGM accepts pixels' pre-readout signals (ϕ_{PRE_READ}) to determine the CG-mode signals, which are also scanned out as 2-bit pixel CGS data. The on-chip pre-ISP receives both CGS data from the CGM module and image data from ADCs. HDR images are produced after the digital gain corrections are completed in the pre-ISP. In comparison to previous designs for adaptive DCG-HDR imaging, neither in-pixel DRAM buffers nor DRAM controllers are needed in the proposed CIS architecture.

III. Chip Implementation

The overall camera architecture is depicted in Fig. 2. The TCG pixel consists of three charge storage nodes (C_{FD}, C_{MCG}, and C_{LCG}), which facilitate three CGs when valve transistors (M_{TX}, M_{MCG} and M_{LCG}) are correspondingly switched on. The column-parallel CGS blocks inside CGM serve the pixel array in a row-by-row basis. Although pixels in each column share the same CGS block, CG-mode signals are determined and accepted by a specific row of pixels selected by the row logic and drivers block. The CGM outputs pixel CGS data to the pre-ISP, which includes a lookup table (LUT) to buffer pixel CGS data for a row of pixels. On the other hand, pixel outputs (ϕ_{PIX_OUT}) are sampled by column-parallel 10-bit single-slope (SS) ADCs, which are in charge of correlated double sampling (CDS) operations and full-bit-depth A/D conversions. All image data are scanned by column scanners and sent to the pre-ISP. For each 10-bit image data, the data conversion block inside the pre-ISP performs gain regulations according to the corresponding pixel CGS data buffered in the LUT. 12-bit HDR data are hereby synthesized to form an HDR image. The CIS chip is controlled and processed by a field-programmable gate array (FPGA) chip, which also hosts a software-based ISP block to accomplish signal processing such as pixel noise compensation, defect pixel correction, and tone mapping.

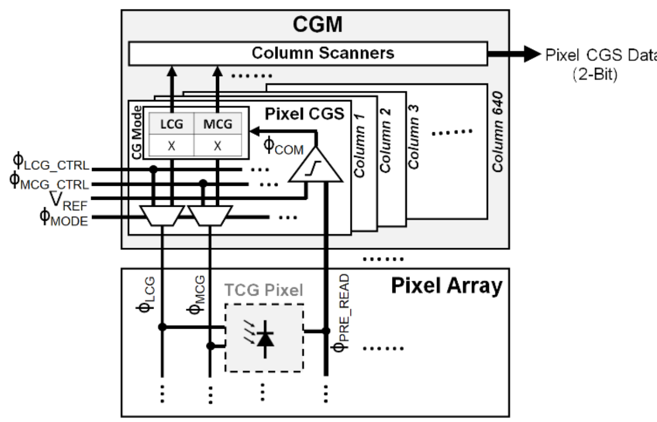

Fig. 3. Block diagram of the CGM module.

Figure 3 shows the block diagram of the CGM module. As mentioned above, the CGS block determines CG-mode signals based on ϕ_{PRE_READ}. A comparator compares ϕ_{PRE_READ} twice with pre-defined reference voltages (V_{REF}). The comparison results (ϕ_{COM}) are stored in a 2-bit CG mode buffer and used as the CG-mode signals. If necessary, the CG-mode signals can be overridden with user-defined CG-mode signals (ϕ_{MCG_CTRL} and ϕ_{LCG_CTRL}). By defining the mode-select signal (ϕ_{MODE}), users have the flexibility to switch off adaptive TCG-

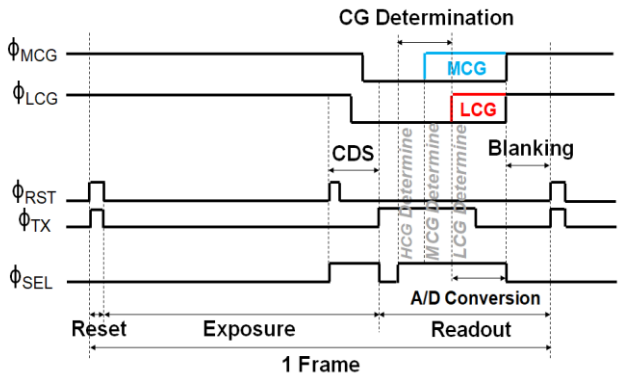

Fig. 4. Timing diagram of a pixel operation.

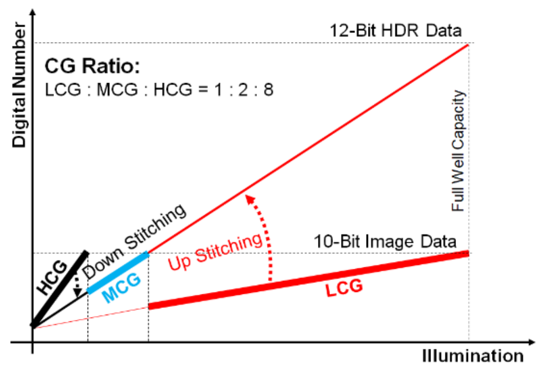

Fig. 5. Gain regulations in adaptive TCG-HDR imaging.

HDR imaging for other types of HDR imaging techniques. A detailed timing diagram of a pixel operation in a frame period is shown in Fig. 4. Pixels are under exposure after being reset at the start of a frame. At the end of exposure period, CG-mode signals and the pixel select signal (ϕ_{SEL}) toggle to implement CDS for noise cancellation. In the readout period, ϕ_{SEL} is pulled up to transfer charges out from the pinned photodiode (PPD). Pixels in the selected row output ϕ_{PRE_READ} to corresponding CGS block for CG determination. Based on the magnitude of ϕ_{PRE_READ}, CG-mode signals toggle to adaptively decide which CG is suitable for ADC operations. Once pixel's CG is determined, ϕ_{SEL} is kept in high and the pixel output (ϕ_{PIX_OUT}) is delivered to ADC for a full-bit-depth A/D conversion. Depending on the speed of image data processing and the frame rate, a blanking period might exist before the start of next frame.

The on-chip pre-ISP preforms data conversions to produce HDR data using the method similar to [5]. The 10-bit image data are regulated with different digital gains according to the CG suggested by their associated pixel CGS data and the CG ratio. As explained in Fig. 5, the 10-bit image data are conditionally stitched up/down and converted to 12-bit HDR data. When the pixel CGS data are '00' (represent HCG), the image data are stitched down. In contrast, the image data are stitched up if the corresponding pixel CGS data are '11' (indicate LCG). No stitching is applied to the image data when the pixel CGS data are '01', which reveal MCG. The

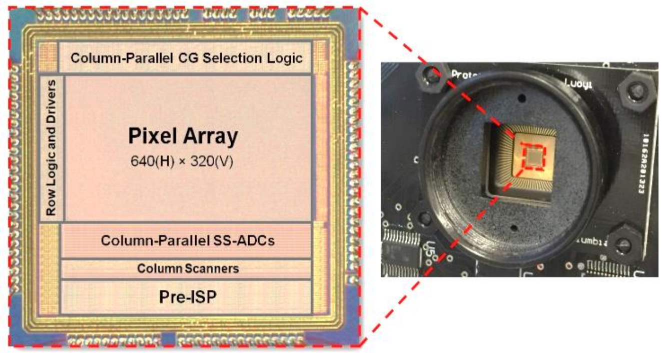

Fig. 6. Chip micrograph (left) and camera module (right).

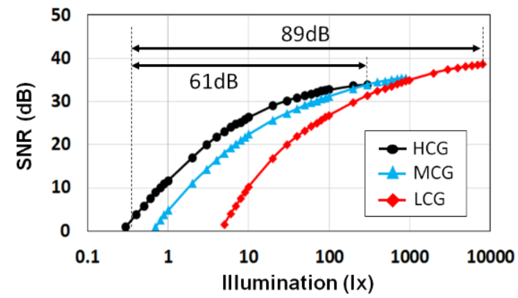

Fig. 7. Measured SNR curves in different CGs.

synthesized 12-bit HDR data are sent out of the CIS chip for further image processing in the FPGA chip.

IV. Experimental Results and Discussion

A prototype CIS chip comprises a pixel array of 640 × 320 TCG pixels is designed and fabricated in a CIS process with a pixel pitch of 5.0µm. The overall chip size is 4.5mm × 4.0mm (including the bonding pads) and the chip micrograph is shown in Fig. 6. The CIS chip was placed on a printed circuit board (PCB) and assembled with a f/1.4 lens as a camera module. The CIS was characterized under the illumination of a D50 light. The measured HCG, MCG, and LCG are 164µV/e-, 42µV/e-, and 23µV/e-, respectively. Therefore, the CG ratio is LCG : MCG : HCG = 1 : 2 : 8. Illustrated in Fig. 7 are the measured signal-to-noise ratio (SNR) curves when operating in single CG modes. The peak SNR in HCG is ~33dB and the dynamic range is 61dB. In combination with MCG and LCG curves, the peak SNR has reached to ~39dB and the dynamic range is extended to 89dB. Note that the CG ratio in this design is relatively small (<1:5), the three SNR curves are linked to each other and SNR dips are neglectable. Although the small CG ratio limits the overall dynamic range expansion, the dip-free SNR profile prevents transition artifacts in HDR images and assures the overall image quality. For future designs, one can further extend the dynamic range by adding more pixel CGs (e.g. ultra HCG (UHCG)) or increasing the CG ratio with risks on image quality deterioration.

The power consumption of the prototype CIS was measured at a frame rate of 60fps and under the full resolution. Concluded in Fig. 8 are the measured chip power in different

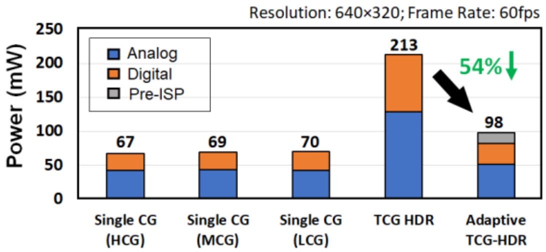

Fig. 8. Measured power consumption in different imaging modes. The on-chip pre-ISP was enabled only in adaptive TCG-HDR imaging.

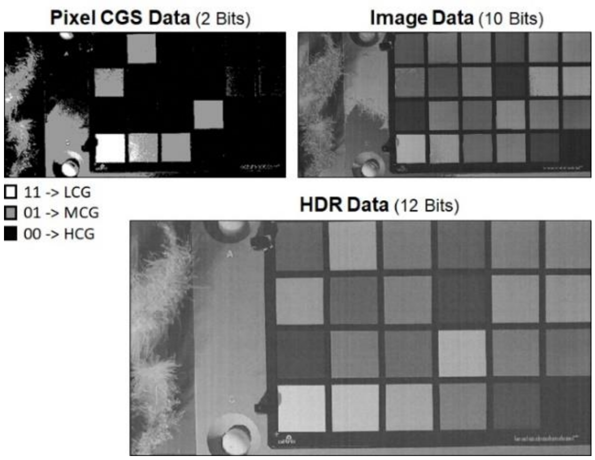

Fig. 9. Captured sample image and the synthesized HDR image in adaptive TCG-HDR imaging.

imaging modes. When forcing all pixels in one of the single CG modes through setting user-defined CG-mode signals, the average power consumed by the CIS chip is ~69mW. If TCG-HDR imaging is applied, the average chip power is 213mW. As pixels are read out three times (each with a different CG) and the ADCs perform three full-bit-depth A/D conversions, it is expected that the overall power consumption in TCG-HDR imaging is three times larger than that in single CG modes. When implementing adaptive TCG-HDR imaging, the CIS consumes 98mW, which is 54% less than that in TCG-HDR imaging. Note that adaptive TCG-HDR imaging costs more power (~29mW) than single CG modes due to the extra power consumed by the on-chip CGM and pre-ISP, which are functionally disabled in single CG modes and TCG-HDR imaging. Figure 9 shows captured sample image data at different stages of applying adaptive TCG-HDR imaging. The pixel CGS data form a 2-bit code map which reveals pixel's CG selections for image readout. By using the pixel CGS data and the corresponding 10-bit image data, HDR data are produced by pre-ISP to form the final HDR image.

Table I depicts a comparison between this work and other related designs for single-frame HDR imaging. The presented CIS chip achieves competitive power figure of merit (FoM) of 7.9nJ/frame·pixel after applying adaptive TCG-HDR imaging. Without including in-pixel buffers and charge modulators, pixels in this work are based on a typical TCG design. Also,

TABLE I
PERFORMANCE COMPARISON

	This Work	**JSSC 2025[5]**	**VLSI 2022 [6]**	**IISW2019[2]**
Process	110nm CIS	350nm CIS	110nm CIS	65nm BSI
Pixel Pitch (μm)	5.0	7.2	7.0	2.8
Pixel Array	640 × 320	512 × 320	320 × 320	1280 × 514
HDR Frame Rate (fps)	60	60	100	30
HDR Power FoM* (nJ/Frame•Pixel)	**7.9 (Adaptive TCG)**	9.9 (Adaptive DCG)	11 (Coded Exposure)	N/A
CG (μV/e-)	164 (HCG) 42 (MCG) 23 (LCG)	228 (HCG) 46 (LCG)	N/A	160 (HCG) 10 (LCG)
CG Ratio	1 : 2 : 8	1 : 5	N/A	1 : 16
Dynamic Range (dB)	61 (Native) 89 (HDR)	63 (Native) 90.5 (HDR)	101.5 (HDR)	>100 (HDR)
Adaptive Tuning	**Yes** (Pixelwise TCG)	Yes (Pixelwise DCG)	Yes (Pixelwise Coded Exposure)	No
In-Pixel Buffer	**No**	Yes (DRAM)	Yes (Storage Diode)	No
Need of Charge Modulation	**No**	No	Yes (2 Taps)	No
On-Chip ISP	**Yes**	No	No	Yes
Applications	**Adaptive TCG-HDR Imaging**	Adaptive DCG-HDR Imaging	Adaptive Temporal HDR Imaging	DCG-HDR Imaging

* Power FoM = (Power)/(Total Pixel Number × Frame Rate)

the pixelwise TCG modulation and the HDR data production are accomplished on chip by the CGM and the pre-ISP to minimize latency in HDR imaging related applications.

V. CONCLUSION

We present a CIS design with pixelwise TCG modulation. According to the scene to be capture, pixel's CG is adaptively determined by on-chip CGM. The pre-ISP collects pixel CGS data and image data to produce HDR images. The proof-of-concept CIS has achieved a dynamic range of 89dB and a dip-free SNR profile. At 60 frames/s, the measured power FoM in applying adaptive TCG-HDR imaging is 7.9nJ/frame·pixel, which is 54% less than that of TCG-HDR imaging. The presented adaptive TCG-HDR imaging is a type of low-power single-frame HDR imaging suitable for mobile cameras.

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